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Fabrication and modeling of thin-film anodic titania memristors

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Fabrication and modeling of thin-film anodic titania memristors

by

Kyle Miller

A thesis submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Major: Electrical Engineering

Program of Study Committee:

Nathan Neihart, Co-Major Professor
Sumit Chaudhary, Co-Major Professor
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Iowa State University

Ames, Iowa

2010

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TABLE OF CONTENTS

LIST OF FIGURES	iv
ACKNOWLEDGEMENTS	vi
ABSTRACT.....	vii
CHAPTER 1. INTRODUCTION	1
CHAPTER 2. REVIEW OF LITERATURE.....	3
2.1 Introduction.....	3
2.2 Switching Mechanisms	6
2.3 Fabrication	12
2.4 Modeling.....	14
2.5 Applications.....	18
2.6 Summary.....	20
CHAPTER 3. METHODS AND PROCEDURES	22
3.1 Introduction.....	22
3.2 Fabrication	22
3.3 Testing.....	24
3.4 Modeling.....	26
3.5 Summary.....	28
CHAPTER 4. RESULTS.....	29

4.1 Keithley Measurement Results	29
4.2 Atomic Force Microscopy Results.....	34
4.3 Ideal Matlab Modeling Results	35
4.4 ORCAD Pspice Memristor Model.....	36
4.5 Summary	40
CHAPTER 5. FUTURE WORK	42
5.1 Memristor Fabrication	42
5.2 Memristor Modeling	43
5.3 Summary	43
APPENDIX A: MATLAB MEMRISTOR MODEL CODE.....	44
A.1 Main Body of Code.....	44
A.2 ODE45 Function Code.....	45
APPENDIX B: VERILOGA MEMRISTOR CODE.....	46
BIBLIOGRAPHY.....	47

LIST OF FIGURES

Figure 1. Figure showing ideal memristor behavior. OFF and ON states shown by (b) and (c) respectively. The operation between states is illustrated in (a).....	5
Figure 2. (a) Unipolar switching and (b) bipolar switching curve examples. Reprinted by permission from Macmillan Publishers Ltd: Nature Materials [4], © 2007.....	6
Figure 3. Formation of a filament in the switching medium for (a) vertical and (b) horizontal structures. Reprinted by permission from Macmillan Publishers Ltd: Nature Materials [4], © 2007.	7
Figure 4. Test vehicle to test TiO ₂ memristor switching mechanisms. Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology [6], © 2008.....	11
Figure 5. Close-up of each junction and a plot of its work function. Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology [6], © 2008.....	11
Figure 6. SPICE Macro Model of a Memristor.	18
Figure 7. Anodization equipment.	23
Figure 8. Example of a finished sample on a titanium film.....	24
Figure 9. Example of sample made with titanium deposited on a glass slide.	24
Figure 10. Probe station with sample under test.....	25
Figure 11. Keithley 4200 Semiconductor Characterization System.....	26
Figure 12. Samples that were not annealed. The number above each plot states how many seconds the sample was anodized for. All currents have been normalized and arrows denote the direction of the sweep.....	30
Figure 13. Annealed samples. The anodization time for each sample is above the respective plot. All currents have been normalized.....	31

Figure 14. Three consecutive sweeps on the not-annealed ten second sample.	32
Figure 15. "Soft-Switching" sweeps for the not-annealed samples.	33
Figure 16. "Soft-Switching" sweeps for annealed samples.	34
Figure 17. AFM images for not-annealed samples. Left to Right: 60s, 10s, 3s, 1s.....	34
Figure 18. Plot made with Matlab memristor model.	36
Figure 19. Comparison of Biolek Pspice model to 10 second sample.....	38
Figure 20. Pspice V vs time memristor model curve.....	39
Figure 21. Pspice I vs time memristor model curve.	40

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ABSTRACT

A new method for the fabrication of memristors is exhibited involving the electrochemical anodization of titanium. This is an inexpensive, room temperature alternative to the current methods of fabrication. Two sets of devices were fabricated with varying anodization times and the devices were characterized. One set of the devices was annealed before characterization to evaluate the importance of annealing as stated in papers. The devices not annealed yielded memristive behavior due to oxygen vacancies created at the titanium-TiO₂ junction buried below the surface of the device. The annealed devices behaved as resistors because the surface of the TiO₂ exposed to the annealing created oxygen vacancies at this interface ensuring both junctions were ohmic. Using an existing model, the best device was modeled by adapting the relevant process parameters.

CHAPTER 1. INTRODUCTION

The memristor is hailed as the missing fourth basic circuit element, and while there are skeptics, the research being done on the memristor is gaining momentum. The device has two terminals and units of resistance. The property that makes the device so unique is the fact that the resistance of the device at any point in time is a function of the current $i(t)$, that has traveled through the device in the past. Another interesting property is revealed once the device is isolated from any potential difference. The resistance value before isolation will be remembered meaning the memristor is non-volatile. A memristor is generally made from a metal-insulator-metal (MIM) sandwich with the insulator usually consisting of a thin film of TiO_2 . One of the reasons the memristor remained hidden for so long is the fact that memristive behavior disappears quickly as the thickness of the thin film is increased above the nanometer scale [1].

Currently, there are few known methods of fabricating the memristor. The most widely used methods are nano-imprint lithography (NIL) and atomic layer deposition (ALD). Both methods require expensive equipment and multiple fabrication steps including a high temperature annealing step and a “forming” step. The literature review will cover these processes, but it is apparent that there is a great need for a cost-effective process to create memristors. The proposed method is anodization of titanium.

Anodization is a well-known process in which an electrolyte is applied to a metal to oxidize it. This forms the cell where the electrolyte is the counter electrode and the metal is the working electrode. A potential difference is applied across the two electrodes with the metal grounded. The applied voltage causes an electrochemical reaction that oxidizes the

metal only while the voltage is applied. Controlling the oxide thickness can be done very easily by varying the time a potential is applied. Making the electrolyte is inexpensive and easy revealing anodization to be a good solution to the problem of fabricating a memristor economically. It remains to be seen whether anodization will need the annealing step, and this will be tested.

A mathematical model for the memristors fabricated using anodization will be presented utilizing one of the newer models found in the literature review. This model could be used to compare process parameters for memristors fabricated using different methods. This will be a good way to evaluate possible strengths and weaknesses of each fabrication process and lead to solutions to fix identified problems. A model can also pave the way for evaluating viability of a circuit containing a memristor without actually having to build the circuit on a bread board to check if the circuit behaves as expected.

Chapter 2 will cover the current state of knowledge regarding the memristor in fabrication, switching mechanisms, modeling and applications. Methods and procedures used to fabricate and characterize the memristors will be described in chapter 3. Chapter 4 covers the findings of the procedures previously described and goes into detail about an explanation of the findings. Possible future directions for this research are described in chapter 5.

CHAPTER 2. REVIEW OF LITERATURE

2.1 Introduction

The memristor was a name coined by Dr. Leon Chua in 1971 when he hypothesized that the memristor or “memory resistor” existed based on an argument of symmetry [2]. He argued that there was no basic passive circuit element to describe the relationship between charge and flux. The capacitor describes the relationship between voltage and charge, the inductor describes the relationship between current and flux, and the resistor describes the relationship between voltage and current. Through this symmetry argument he wrote equations that described how the memristor would behave and found it had units of resistance but the device’s resistance depended on the history of current that had previously flowed through the device; hence the name.

Many papers that show memristive behavior were published long before the memristor was actually discovered (which didn’t happen until 2008). The authors of these papers did not realize that the behavior witnessed was memristance. One such paper by Hickmott [3], published in 1962, observed an odd negative resistance in thin oxide films in the realm of one nanometer thick. The purpose of the paper was to characterize oxide films in the realm of 150 to 1000 Å thick as these films had no application yet and were ignored in research. Aluminum, tantalum, titanium, and zirconium were all anodized to grow the desired thickness of oxide and then characterized. Characterization consisted of sweeping the voltage on each oxide film. The results show that there is a critical voltage where the conductivity of the film greatly increases which is not breakdown. The first time this is done

the current is very erratic, but on successive voltage sweeps the current stabilizes. An irreversible change has occurred in the oxide and the term “forming” is used to describe the first voltage sweep that permanently increases the conductivity of the oxide film. Lowering the voltage across the same film resulted in a region of negative resistance. All oxides tested in this paper showed negative resistance, but aluminum, reportedly, showed negative resistance more readily. Negative resistance is accredited to the tunneling of electrons at an extremely rapid rate.

It was not until 2008 that the physical implementation of the memristor was discovered by Strukov et al. [1]. Their memristor was made using annealed TiO_2 . Annealing is a process of baking a material, usually for the purpose of making an amorphous material restructure to a crystal. In this case, annealing is used to create oxygen vacancies. The heat from annealing gives the oxygen enough energy to escape the TiO_2 bonds. The annealing is completed in an atmosphere of hydrogen so that any escaped oxygen will bond with the hydrogen to create water vapor. Oxygen vacancies are fundamental to the operation of the memristor, as will be described later. Strukov et al. [1] gave a good ideal description of how the actual memristor behaves.

Equations (1) and (2) describe the ideal memristor and create an ideal mathematical model.

$$v(t) = \left(\frac{R_{ON}w(t)}{D} + R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right) i(t) \quad (1)$$

$$\frac{dw(t)}{dt} = \frac{\mu_V R_{ON}}{D} i(t) \quad (2)$$

The voltage across the terminals and the current through the device are given by the variables $v(t)$ and $i(t)$. The thickness of the switching medium (TiO_2) is a constant described by D . The thickness of the switching medium that is saturated with oxygen vacancies which assist conduction is described by the function $w(t)$. The lowest and highest resistances that the memristor can attain are R_{ON} and R_{OFF} respectively. The mobility of the oxygen vacancies is given by μ_v and is known to be $10 \text{ fm}^2/(\text{Vs})$. Fig. 1 shows an illustration of how the equations work. The doped region corresponds to the annealed TiO_2 (TiO_{2-x} which represents reduced TiO_2) while the undoped region represents the part of the TiO_2 that was too deep and not affected by the annealing. If a positive voltage is applied to the doped side, the vacancies being positively charged will be repelled and drift into the undoped region restricted by the mobility of the oxygen vacancies given by μ_v . Eventually w will become equal to D resulting in the ON state as shown in Fig. 1. If the bias voltage is swapped, the oxygen vacancies will recede. Eventually w will be equal to 0 resulting in the OFF state as the vacancies are completely pushed to one side. This behavior shows that the restriction on w is that it can never be greater than D or less than 0. Unfortunately (1) and (2) have no boundary conditions defined to restrict w to this region.

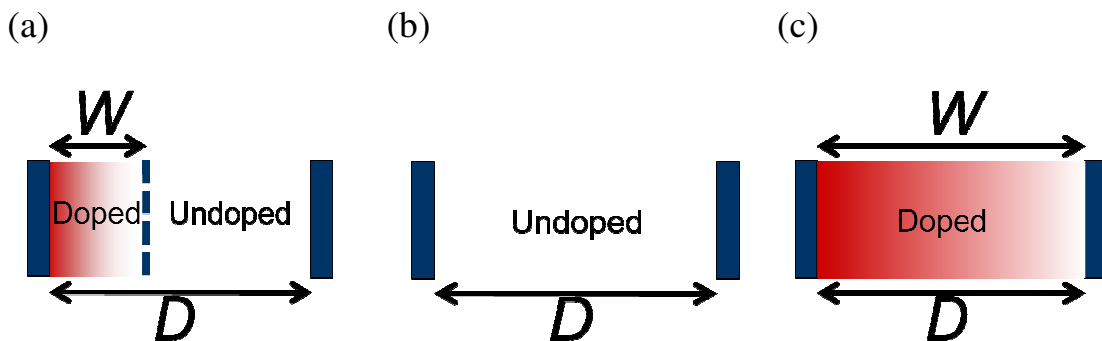


Figure 1. Figure showing ideal memristor behavior. OFF and ON states shown by (b) and (c) respectively. The operation between states is illustrated in (a).

2.2 Switching Mechanisms

The two methods of switching in resistive switching memories are by cation/anion migration or formation of a filament. These mechanisms for switching are described in detail and called unipolar or bipolar switching by Waser and Aono [4]. Switching is unipolar if the switching procedure is not dependent on the polarity of the voltage and current signal. A system in the OFF state is switched by a voltage threshold to the ON state and the current is limited by the compliance. Resetting back to the OFF state happens at a voltage below the on threshold but does not have to be negative. A much higher current is observed for switching to the OFF state, and Fig. 2(a) displays an example of a unipolar curve. Fig. 2(b) shows a bipolar curve. Bipolar switching is characterized by the ON state occurring at a voltage threshold and the OFF state at the opposite polarity.

Now that the criteria for both types of switching behavior is understood, it is time to discuss where in the oxide the switching mechanism is occurring and what is causing it. Reportedly, switching to the ON state is confined to a filament rather than spread across the

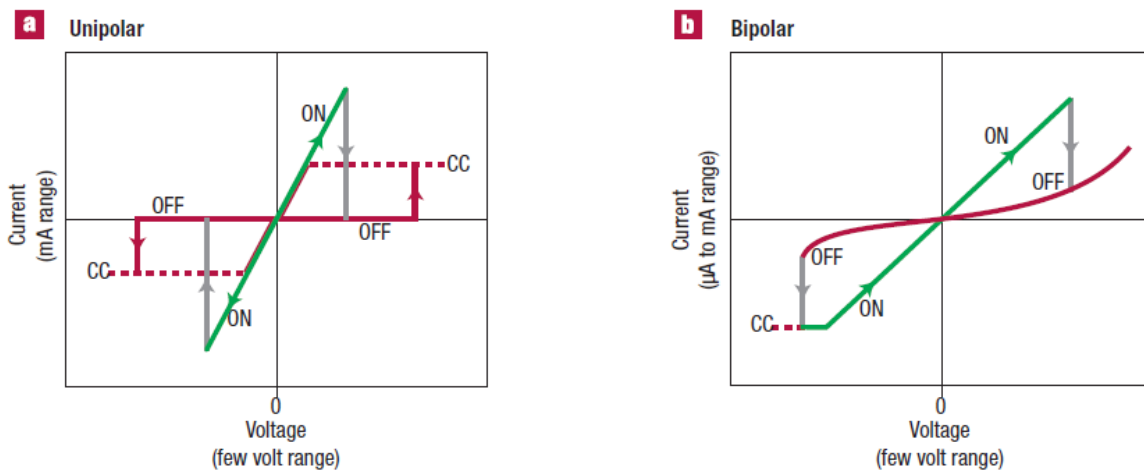


Figure 2. (a) Unipolar switching and (b) bipolar switching curve examples. Reprinted by permission from Macmillan Publishers Ltd: Nature Materials [4], © 2007.

entire pad or contact [4]. This behavior has led to a resistance completely independent of the pad or contact size. Fig. 3 demonstrates a vertical and lateral configuration for the metal-insulator-metal (MIM) sandwich. The red filament is the filament responsible for the change in states.

The actual mechanisms that promote switching can be classified as thermal, electronic or ionic [4]. Thermal switching shows unipolar switching and is initiated by partial dielectric voltage breakdown where the material in a discharge filament is modified by Joule heating. Due to the compliance current, only a weak conductive filament forms composed of electrode metal, carbon from residual organics, or decomposed insulator material. During reset, the filament is disrupted thermally because of high power density on the order of 10^{12} W/cm³ leading to the fuse-antifuse name for this mechanism. TiO₂ specifically can show bipolar switching, but it can be changed to a unipolar switching characteristic by setting the compliance high enough without breakdown occurring.

Electronic charge injection is another mechanism where charges are injected through

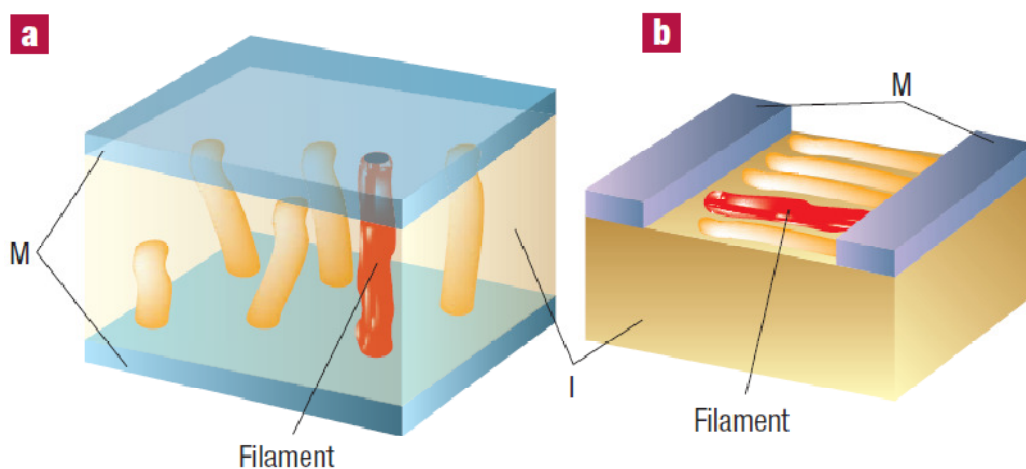


Figure 3. Formation of a filament in the switching medium for (a) vertical and (b) horizontal structures. Reprinted by permission from Macmillan Publishers Ltd: Nature Materials [4], © 2007.

tunneling and trapped at defects or metal nanoparticles in the insulator. These trapped charges are dispersed throughout the insulator reducing the resistance to the ON state. Waser and Aono focus on the ionic transport and redox reactions which yield bipolar switching [4]. In MIM systems, metal cations in the ionic conductors migrate to the cathode of inert materials and are reduced. The reduced metal atoms form a metal filament that grows towards the anode lowering the resistance to the ON state. Changing the polarity of the bias voltage dissolves the metal atoms at the edge of the filament thus destroying it and raising the resistance to the OFF state. This is an example of cation migration. Bipolar switching in transition metal oxides happens because of oxygen ion defects, typically oxygen vacancies. This is an example of anion migration and oxygen vacancies typically have a higher mobility than cations. If the cathode blocks ion exchange reactions during a forming process, an oxygen-deficient region can expand towards the anode eventually forming a conducting filament. If the anode is reactive, it can be oxidized as a side-effect of this switching process.

For TiO_2 specifically there has been a paper that delves into the resistance switching mechanism of a thin film grown by atomic-layer deposition (ALD) [5]. The films were grown using $\text{Ti}(\text{OC}_3\text{H}_7)_4$ and O_3 as a precursor and oxidant, respectively. The $\text{Ru}/\text{SiO}_2/\text{Si}$ wafer was kept at 250°C and the TiO_2 film thickness was varied between 20 nm and 57 nm by adding deposition cycles. The films grown showed a polycrystalline microstructure with a rutile crystal structure. Platinum and aluminum were used for the top electrodes with a 300 mm diameter and deposited by electron-beam evaporation. The virgin samples showed a resistance of $10^9 \Omega$ for -1 V to 1 V sweeps. To lower the resistance and facilitate the desired switching behavior, a voltage of 2.2V was applied for the 57 nm films with a proper current compliance for soft-breakdown. The current compliance is extremely important because a

current in the realm of 70 mA would cause hard-breakdown and destroy the device. After this forming step, the film remains in the on state for both negative and positive biases. Increasing the bias voltage causes an increase in the current density until the density suddenly drops to a very low value at a voltage threshold turning the device off. This switching occurs at both polarities and further increasing the bias voltage above 1.5V causes the device to recover the ON state. As long as the bias voltage is limited below both thresholds, the ON and OFF states are not disturbed after a few hundred readings. The devices with platinum for the top contact showed resistance switching regardless of bias polarity. The aluminum devices however, showed switching behavior only if the positive bias was applied to the top electrode. The actual switching mechanism must be understood to explain this behavior. One probable model for the formation of linear conducting paths is the formation of conducting filaments. Filaments are one of the specific forms of extended defects in insulating ionic crystals and many extended defects occur along grain boundaries of polycrystalline samples. These extended defects exhibit local conductivity greater than a few orders of magnitude more compared to the rest of the switching medium. When ionic oxide crystals like TiO_2 are reduced, oxygen vacancies form and drift under an applied electric field. The oxygen is allowed to escape the switching medium through the platinum top electrode as it is inert and has a high mobility. If the device has an aluminum top contact, it is reactive and the oxygen will oxidize the aluminum. This hypothesis was verified by wet-etching the aluminum with nitric acid, and witnessing aluminum oxide left near the TiO_2 boundary. The initial forming process was responsible for the reduction of TiO_2 and forcing oxygen ions into the top electrode. When a negative bias is applied, the vacancies drift away from the top electrode and escape into the atmosphere if the contact is platinum. At the

threshold voltage the defects generated by the forming process align forming a conducting filament facilitating the ON state. The off state is regained by destruction of the filament due to increasing current that causes thermal rupture. Conductive atomic force microscopy (CAFM) carried out by etching away the contacts after a state was programmed affirm the filament hypothesis by showing tiny spots of high conduction during the conductivity map.

After the memristor was discovered, investigation by Yang et al. [6] was done into what mechanisms actually were at work in a memristor, as the previously described papers did not look at the work functions of each contact. In order to observe the switching mechanisms at work a specialized test platform was fabricated. A single crystal substrate of rutile TiO_2 was annealed in a 95% N_2 and 5% H_2 gas mixture at 550°C for 2 hours to create an oxygen-deficient layer at the surface. Titanium 5 nm thick was then deposited onto the substrate to further reduce the oxide and increase vacancies (shown by TiO_{2-x} region). Platinum pads 80 nm thick were deposited on the TiO_2 substrate and on top of the titanium thin film. The test vehicle is displayed in Fig. 4. Metal/semiconductor contacts are known to be ohmic if the semiconductor is heavily doped and Schottky rectifying in the case of low doping concentrations. The titanium/ TiO_{2-x} (indicates reduced TiO_2 which will contain oxygen vacancies) junction should be ohmic because of the high concentration of oxygen vacancies and the platinum/ TiO_2 interface should be Schottky rectifying as shown in Fig. 5. Fig. 5 was verified by sweeping the voltage between pads 1 and 4 and finding an exponential relationship with the current as expected with a Schottky rectifier. Sweeping the voltage between pads 2 and 3 showed a linear relationship as expected with ohmic contacts.

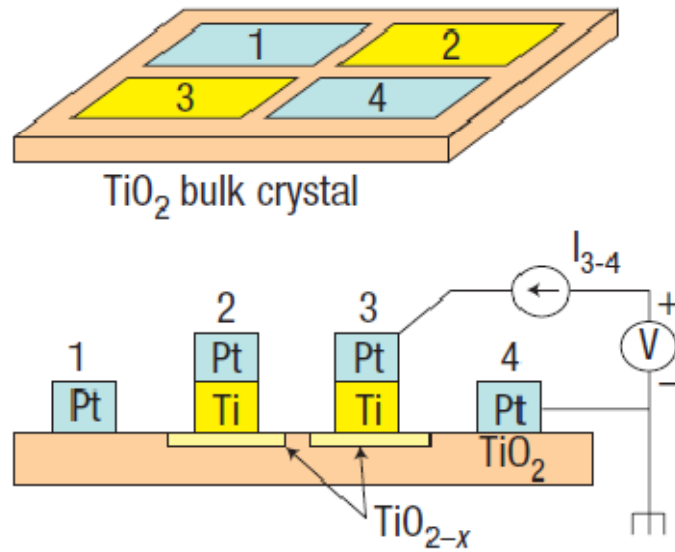


Figure 4. Test vehicle to test TiO_2 memristor switching mechanisms. Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology [6]. © 2008.

The investigation found that if a positive bias was applied to pad 3 and pad 4 was grounded, the oxygen vacancies migrated to the Pt/ TiO_2 barrier eventually forming the low resistance state. Applying a positive bias to pad 4 at this point will repel the oxygen vacancies back to the titanium contact recovering the high resistance state [6]. This is anion migration also known as bipolar switching [4]. To verify whether conduction was localized to filaments as observed in the previously mentioned papers, pad 4 was cut in half to see if

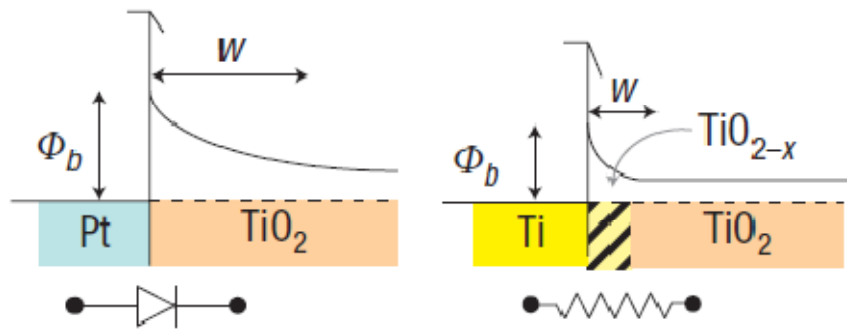


Figure 5. Close-up of each junction and a plot of its work function. Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology [6], © 2008.

both halves would still show resistance switching behavior. Only one of the pad halves showed switching demonstrating that conduction was localized instead of uniform.

2.3 Fabrication

A memristor can be made from any Metal Insulator Metal (MIM) sandwich which exhibits a bipolar switching characteristic. This suggests that TiO_2 is not the only material to fit the criteria for a memristor, and there has been a few papers published on the fabrication and properties of memristors fabricated using other materials. Even if the same materials are used, there are different methods of fabricating memristors. So far the most common methods are nano-imprint lithography (NIL) [7], [8] and atomic-layer deposition (ALD) [5], [6]. Both of these processes require an annealing step at high temperature and a forming voltage [3], [5], [6], [9].

One such paper by Stewart et al. [10] explores the possibility of using an organic monolayer as the switching medium to realize a memristor. Two terminal devices were fabricated using sequential deposition of titanium followed by the organic Langmuir-Blodgett (LB) monolayer, and finally the platinum top contact was deposited. The devices were fabricated in crossbar arrays on top of silicon wafers with an oxide thickness of 200 nm. Eicosanoic acid, rotaxane, and rotaxane missing the interlocked tetracationic cyclophane ring were the LB monolayers studied. Through testing, it was observed that any voltages between -2 V and 1 V resulted in an exponential I - V relationship generally related to direct tunneling through a film of 2.5 nm. If the voltage was raised higher, an irreversible change to a bipolar switching state was recorded. This was dubbed the “forming” step and all behavior reported describes the devices after the forming step. All three LB monolayers exhibited the

characteristic memristive “figure-8” I - V curve and when tested with repeated sweeps that stayed positive for the duration of the sweep, each successive sweep yielded a larger current than the last showcasing these devices inherently had some type of memory.

Lu et al. describes a CMOS compatible memristor using amorphous silicon as the switching medium [9]. The switching occurs in an amorphous silicon device through formation and destruction of a metal filament from one of the contacts that pierce into the switching medium. To achieve the described switching behavior, a forming voltage was applied. This forming voltage often destroys the device. Fabricating the amorphous silicon device with a bottom contact made using silicon heavily doped with positive carriers decreases the voltage of the required forming process increasing yield. Fabrication of the amorphous silicon layer was done with plasma-enhanced chemical vapor deposition (PECVD) and low-pressure chemical vapor deposition (LPCVD). Different metals were used for the top contact, and memristive behavior was observed in all cases. Using the unique device structure described, only two of more than three hundred devices characterized did not exhibit resistive switching behavior. Scalability of the devices was also tested down to 50 nm x 50 nm. The resistance of the on-state increased by 2.5 times when the device area was reduced 6 orders of magnitude. Switching speed was also characterized and 5 ns was generally achieved with the LPCVD devices while PECVD devices only saw speeds limited to 150 ns due to the higher intrinsic resistance. After programming a state, little degradation of the stored state was seen after more than five months at room temperature in ambient air. The endurance of the amorphous silicon devices was also characterized by repeatedly programming each device. The on-state resistance did continually increase, but switching was reliable after 10^6 cycles if a low switching current is used.

The most unique fabrication process presented was a method of fabricating a memristor on a flexible polymer [11]. The fabrication process involved spinning a titanium isopropoxide solution onto the polymer substrate for sixty seconds to create a uniform thin film of amorphous TiO_2 60 nm thick after hydrolyzing in air for one hour. The bottom contact of 80 nm aluminum is deposited on the polymer substrate before spinning the gel. The top contact is also 80 nm aluminum deposited after the solution has formed the oxide. Both contacts were deposited using thermal evaporation through a shadow mask. Using this method, the authors have achieved a physically flexible memristor with a cheap fabrication process at room temperature. The operation voltages are less than ten volts which is low voltage for flexible electronics. They achieved on/off ratios greater than 10,000:1, memory retention of over 1.2×10^6 seconds, and reliability after bending the device 4,000 times. Fifty devices were fabricated and forty-two exhibited the desired bipolar switching behavior.

2.4 Modeling

Strukov et al. [1] included some basic equations for a very ideal model of the memristor, but they did not address the fact that near the contacts of the memristor dopant drift slows down a lot due to boundary effects. An actual memristor is, of course, not ideal and not well described by (1) and (2). The vacancies actually tend to drift along grain boundaries in the crystal forming little filaments of conduction that short out the Schottky rectifying contact [6]. As the oxygen vacancies approach either boundary of the switching medium, their drift slows considerably due to the limitation that w can never be less than 0 or greater than D resulting in a nonlinear drift phenomenon [12].

Joglekar and Wolf [12] have developed a mathematical model for the nonlinear drift of the oxygen vacancies. The paper introduces the ideal memristor model and then dives into some ideal modeling of circuits containing combinations of memristors, capacitors, and inductors. To account for the nonlinear drift, a windowing function can be used to restrict the value of w to be greater than 0 and less than D . Equation (3) should replace (2) in the ideal model to account for nonlinear drift.

$$\frac{dw}{dt} = \frac{\mu_V R_{ON}}{D} i(t) F\left(\frac{w}{D}\right) \quad (3)$$

Where the window function $F(w/D)$ is given by:

$$F\left(\frac{w}{D}\right) = 1 - \left(2\frac{w}{D} - 1\right)^{2p} \quad (4)$$

The constant p parameterizes a family of window functions and is a positive integer. As p is increased, the amount that the mobility of the oxygen vacancies is hampered decreases considerably up to a p of ten except for when w is near 0 or D . Near these boundaries, mobility is greatly reduced achieving the desired behavior.

Biolek et al. [13] builds on the windowing function proposed by Joglekar and implements it into a PSPICE model as a subcircuit that can easily be brought into the PSPICE program and used to simulate the memristor. The paper goes on to point out problems with the current approach to modeling the boundary effects using windowing functions. If the memristor is set to the terminal state ON or OFF, no external stimulus can change the state. This is because of the zero value of the windowing function at either boundary. The current window function models the memristor as a component that remembers the amount of electric charge that has passed through it, but the resistance actually depends upon the location of the oxygen vacancies in the switching medium. These

problems can be resolved by designing a window function which models the fact that the boundary speeds of approaching and receding from the boundaries are different. Equation (5) presents the proposed window function to resolve these issues.

$$f\left(\frac{w}{D}\right) = 1 - \left(\frac{w}{D} - \text{stp}(-i)\right)^{2p} \quad (5)$$

Equation (5) does not model the hard switching effects governed by nonlinear ionic drift characterized by a symmetrical hysteresis loop as well as Joglekar's window function. The memristor current is represented by i .

Strukov et al. [14] published another paper in 2009 to better model the nonlinear behavior of the memristor and expand upon the ideal equations presented in the first paper. This more physical model of the memristor is based on numerical solutions of coupled drift-diffusion equations for electrons, holes, and ions to simulate the dynamics of two terminal devices based on a MIM structure. The model assumes the memristor is a one-dimensional device that has a semiconductor thin film containing charged, mobile n-type dopants with concentration $N_D(x)$ confined by electrodes at $x=0$ and $x=L$. Both donors and acceptors are assumed to be shallow and only bulk limited transport is considered.

$$\nabla \cdot (-e * n(x) \mu_n \nabla \phi_n(x)) = 0 \quad (6)$$

$$\nabla \cdot (-e * p(x) \mu_p \nabla \phi_p(x)) = 0 \quad (7)$$

$$-\epsilon \epsilon_0 \Delta \phi(x) = e(p(x) - n(x) + f_D(x) N_D(x) - f_A(x) N_A) \quad (8)$$

$$J_{ION}(x) = -e D_i \nabla N_D(x) - e N_D(x) u_i \nabla \phi(x) \quad (9)$$

$$\frac{e \partial N_D(x)}{\partial t} = -\nabla \cdot J_{ION}(x) \quad (10)$$

In (6)-(10), $n(x)$ and $p(x)$ represent the electron and hole concentrations respectively. The quasi-Fermi potentials are represented by ϕ_n and ϕ_p . The unit charge is given by e , $\varphi(x)$ is the electrostatic potential, μ_n is the electron mobility, μ_p is the hole mobility, $f_D(x)$ is the ionization factor for donors, $f_A(x)$ is the ionization factor for acceptors, $J_{ION}(x)$ is the mobile ion distribution and ion flux, D_i is the ion diffusion constant, $\epsilon\epsilon_0$ is the permittivity of the active layer, and μ_i is the ion mobility. The boundary conditions are:

$$\phi_n(0) = \phi_p(0) \quad (11)$$

$$\phi_n(L) = \phi_p(L) = \phi_n(0) + v \quad (12)$$

$$J_{ION}(0) = J_{ION}(L) = 0 \quad (13)$$

In (12), v is an applied bias. Using the above equations to create a model, it can be proven that a state variable cannot emulate the dynamical evolution of the resistance of the system [14]. This implies that any mathematical models that depend on a state variable will not be able to properly represent the hysteresis of the resistance in the memristor.

Kavehei et al. [15] takes a fresh look at all of the research done so far on the memristor. The most interesting part for this thesis is the discussion on modeling nonlinear drift. So far all papers have put forth some sort of a window function to resolve the boundary conditions of the memristor. It is postulated in [15] that all these window functions fail because they only depend on the state variable x , and as mentioned in [14], "There is not a single state variable that describes the dynamical evolution of the resistance of the system." To address this issue, a new SPICE macro model is proposed that is claimed to be the best model of memristor behavior so far, shown in Fig. 6.

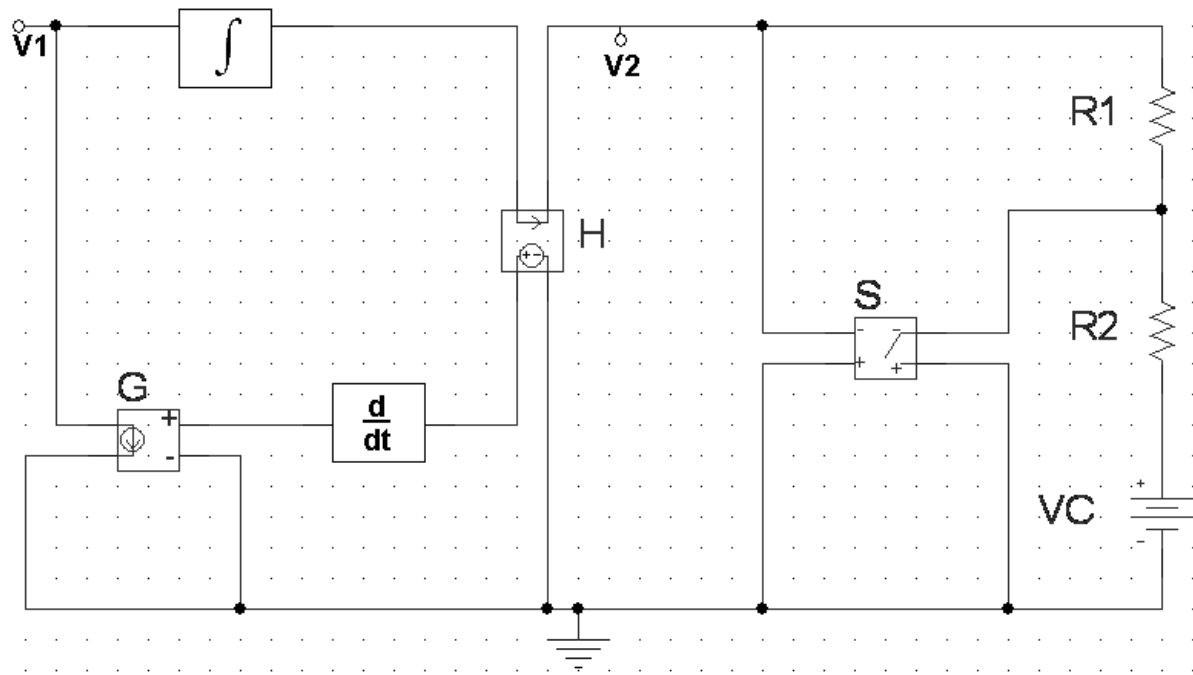


Figure 6. SPICE Macro Model of a Memristor.

2.5 Applications

The discovery of memristors has yielded a new device, but now engineers and scientists alike scramble to find applications. Tweaking old circuit configurations by adding a memristor or using the properties of the memristor to come up with a new innovative architecture will be commonplace. The first application that will most likely see widespread use will be memristors utilized as non-volatile memory. There are already a couple of papers that demonstrate memristors being utilized in a dense crossbar array to make memory [16].

Jo et al. [16] expanded upon the amorphous silicon memristor they created and built it into a massive crossbar memory array capable of storing 1 kb of data. The memory density is 2 Gbits/cm² and the width of the lines in the crossbar is just 120 nm. The yield for the array was 98%. The Ag/a-Si/p-Si devices used showed programmability for more than 10⁵

writing cycles. Each bit was written with a 5.5 V pulse to store a conductivity of 200 μS , but there is no indication of the speed at which the array can be written or read in the paper.

Another creative application for crossbar array of memristors is put forward in Xia et al. [8]. This paper introduces an idea to make field programmable gate arrays (FPGA) more dense by fabricating all the logic gates using standard CMOS processes on a wafer and then depositing a memristor crossbar array on top of the wafer to handle all of the interconnections. The idea was tested through fabrication in a 0.5 μm technology. A 1 μm thick layer of SiO_2 was deposited on top of the completed wafer and planarized to expose the tungsten vias that are used to connect the crossbar wires of the memristor array. NIL would be used to create the crossbar on top of the wafer, but depressions in the surface required an extra planarization step using a layer of NIL resist flattened with a quartz plate. Once the bottom contacts were deposited with NIL, TiO_2 was deposited over the entire wafer to create the switching medium for the memristor crossbar array. The top wires were again created using NIL with 100 nm thick wires. This process created memristors with 100 x 100 nm^2 junction area, 36 nm thick TiO_2 switching layer, 9 nm thick platinum bottom contact, and 12 nm thick platinum top contacts. The FPGA was tested by configuring the logic to a known state and testing the truth table. The results from the fabricated FPGA show that the memristors were configured correctly, the transistors in the CMOS layer were successfully connected by the memristors, and the fabrication process for building memristors on top of a wafer did not disturb the underlying logic.

Just the concept of memristance itself has proven useful in modeling very non-linear systems. One such system is the neuron which has fueled research into learning and modeling behavior of biological creatures [17]. One such creature was an amoeba that was

subjected to a change in temperature at regular intervals and scientists measured the response of the amoeba to the stimulus. The amoeba reduced movement when a drop in temperature occurred, so scientists applied the same drop in temperature at a certain frequency for awhile and suddenly stopped changing the temperature. They found that the amoeba learned the frequency and continued to slow its speed in preparation for the drop in temperature even if it did not occur. A simple memristor circuit was used to model the amoeba being exposed to the same stimuli and learning the pattern [18]. It was also shown that if the pattern was disturbed before it had been completely learned, both the amoeba and the memristor circuit would not learn the pattern.

A neural network of memristors was also used to demonstrate associative memory [19]. This was done by creating a memristor emulator that consisted of a digital potentiometer, an analog-to-digital converter (ADC), and a microcontroller programmed to behave like a memristor. A neural network is built with this emulator so that one neuron is for the sight of food, one is for sound, and another for salivation. Stimulating the sight neuron yielded salivation as expected. Stimuli to the sound neuron did not trigger salivation. The goal was to program the memristor neurons so that the sound would be associated with sight and trigger salivation; hence associative memory. The memristor circuit was able to model associative memory and “learn” to associate sight with sound.

2.6 Summary

Current and past research was split into four main categories which were switching mechanisms, fabrication, modeling, and applications. Switching mechanisms dealt with how a memristor’s resistance changed and why. From the explored papers, it seems that the

mechanisms that make memristors work are well understood. Fabrication of memristors looked at different methods and materials used to create a memristor. Since most MIM systems are capable of some sort of switching behavior, there seems to be a lot of unexplored territory in this area of research. Modeling takes understanding the switching mechanisms to the next level and applies mathematics to imitate the memristor's behavior for a given applied current or voltage. The main problem that multiple papers attempted to address was the non-linear drift phenomenon. The latest paper may have fixed most of the issues with the previous attempts to model the oxygen vacancy drift, but modeling the memristor is still in its infant stages with much more work to be done. Even though it has not been long since the discovery of the memristor, people have already come up with some clever applications for the memristor. Much of the focus of this research area has been using the memristor as a memory or a switch, but as the other three research areas advance, the applications for the memristor will grow immensely.

CHAPTER 3. METHODS AND PROCEDURES

3.1 Introduction

The following chapter details the methods and procedures detailing the fabrication of memristors using anodization of titanium. Anodization involves utilizing an electrolyte to grow an oxide with the help of an applied electric potential. Procedures are also described for testing the samples and for creating a model of the memristor to imitate the behavior of the anodized samples.

3.2 Fabrication

To create a smooth, uniform substrate to anodize, titanium was evaporated using an electron-beam and deposited in a layer ~500 nm thick onto a glass slide. These glass slides were then clamped in an apparatus that exposed about 1 cm² circular area of the titanium for anodization. The top half of the apparatus had a hole with an o-ring to hold the electrolyte that would be used for the anodization as shown in Fig. 7.

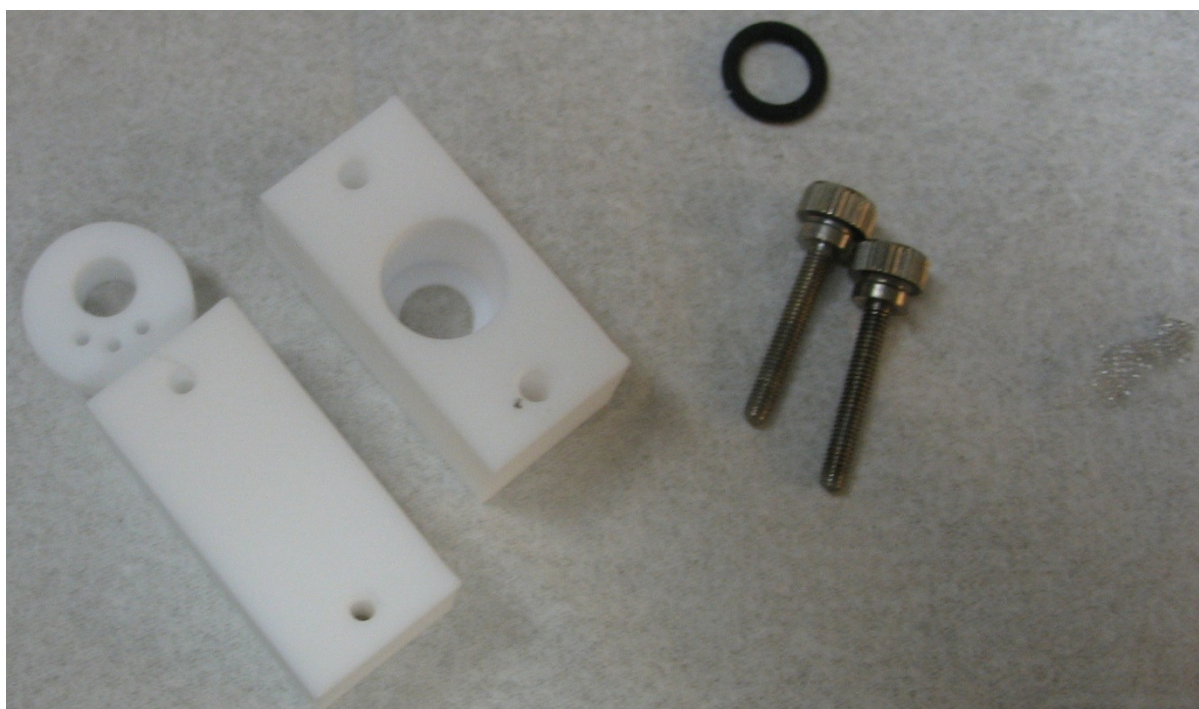


Figure 7. Anodization equipment.

The electrolyte itself consisted of a 0.27 M NH_4F mixture in a volumetric ratio of 16.7:83.3. The anodization was performed at a constant potential of 30 V with the Ti substrate serving as the anode and a platinum mesh dipped in the electrolyte as the cathode. To fabricate different oxide thicknesses for experimentation, the time the 30 V was applied was varied. For the following experiment, anodization times of 1, 3, 10, and 60 seconds were used. Two sets of identical samples were made to verify if this new process also required annealing like others. Annealing was done on one set of samples at 550°C for one hour in a 96% N_2 and 4% H_2 atmosphere. The bottom contact was simply the titanium not exposed to the electrolyte. To create the top contact, dots of silver paste were applied to the newly grown oxide to create many different sites to test on one sample. Silver was an ideal material for the top contact as silver is inert and would not react with any escaping oxygen. Fig. 8 and 9 show examples of newer samples with 100 nm thick palladium pads deposited on top.

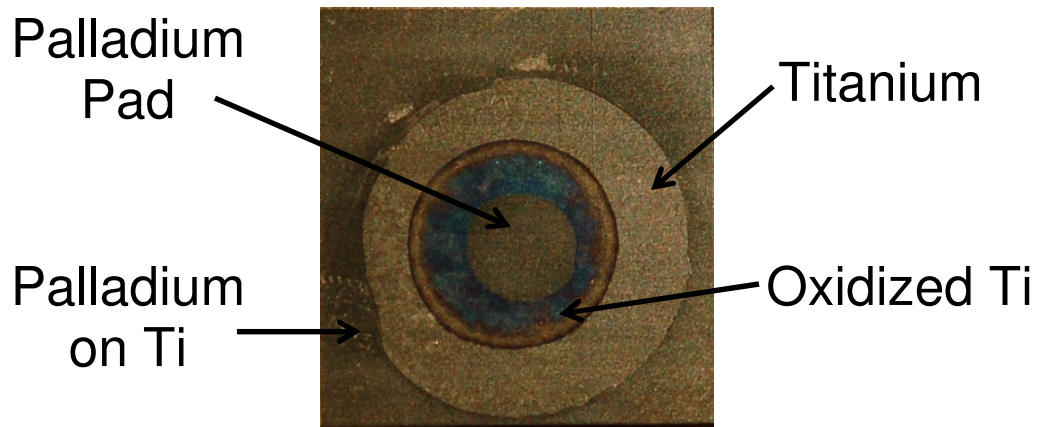


Figure 8. Example of a finished sample on a titanium film.

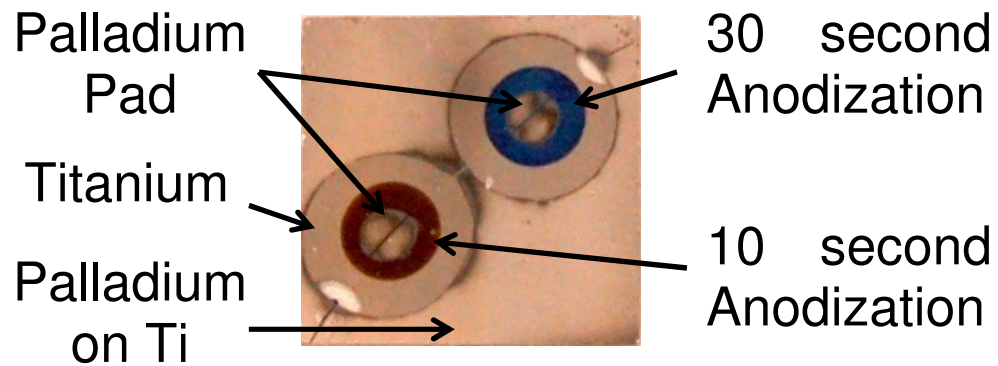


Figure 9. Example of sample made with titanium deposited on a glass slide.

3.3 Testing

The same tests were applied to both annealed and regular samples. The Keithley 4200 semiconductor characterization system connected to a probe station was used to characterize the samples. The probe station setup is pictured in Fig. 10 while the Keithley 4200 semiconductor characterization system is displayed in Fig. 11.

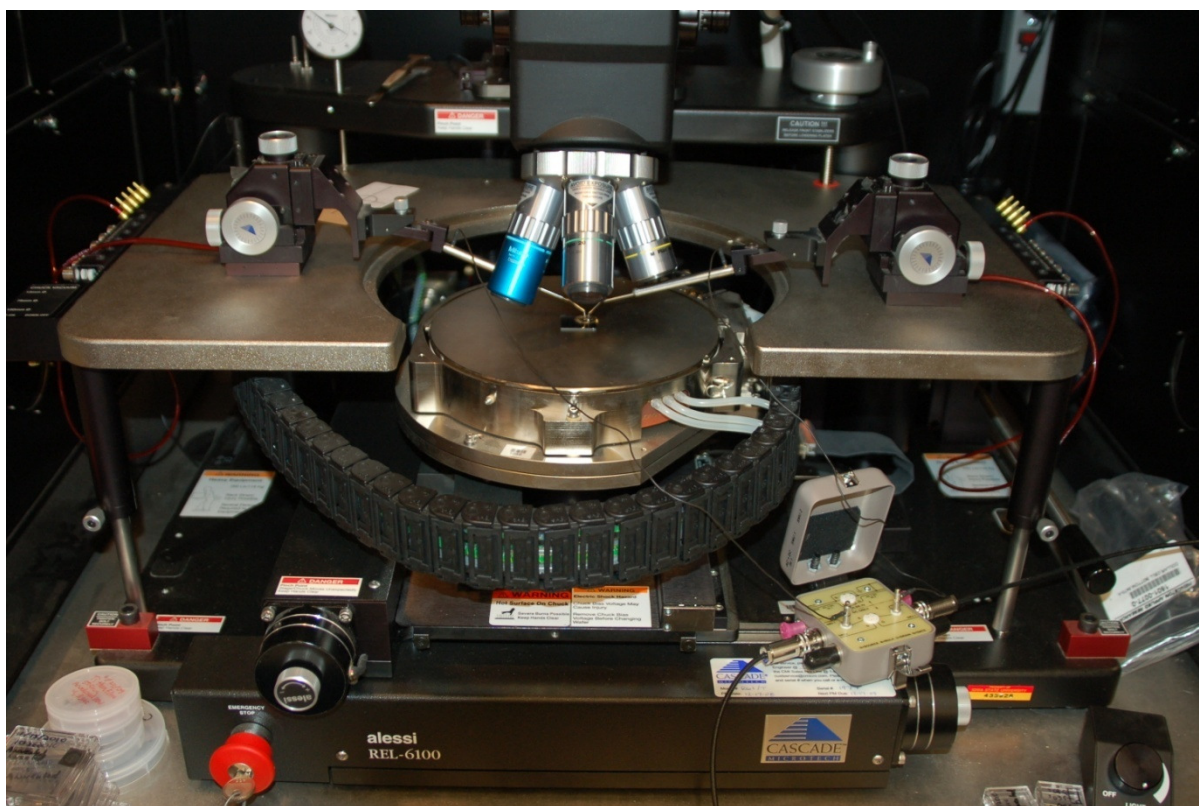


Figure 10. Probe station with sample under test.

The bottom titanium contact was grounded for all measurements, and silver paste applied to the oxidized titanium was used as a forcing node. A forming voltage of 8 V with a 0.1 A current limit was first applied because of the number of papers citing its necessity. Only measurements using a varying DC bias voltage were completed. The first test started at 0 V, climbed up to 1 V, fell down to -1 V and rose back up to 0 V called the “figure-8” sweep. Eighty-three data points were taken in total and the whole sweep took approximately 8 seconds. This test was chosen to show the bipolar switching characteristics of a memristive device. The other test was just a repeated sweep from 0 V up to 1 V and back to 0 V called “soft-switching” sweep. For this sweep approximately 200 points were taken. The purpose of the “soft-switching” sweep was to not sweep negative and repeat the test multiple times in

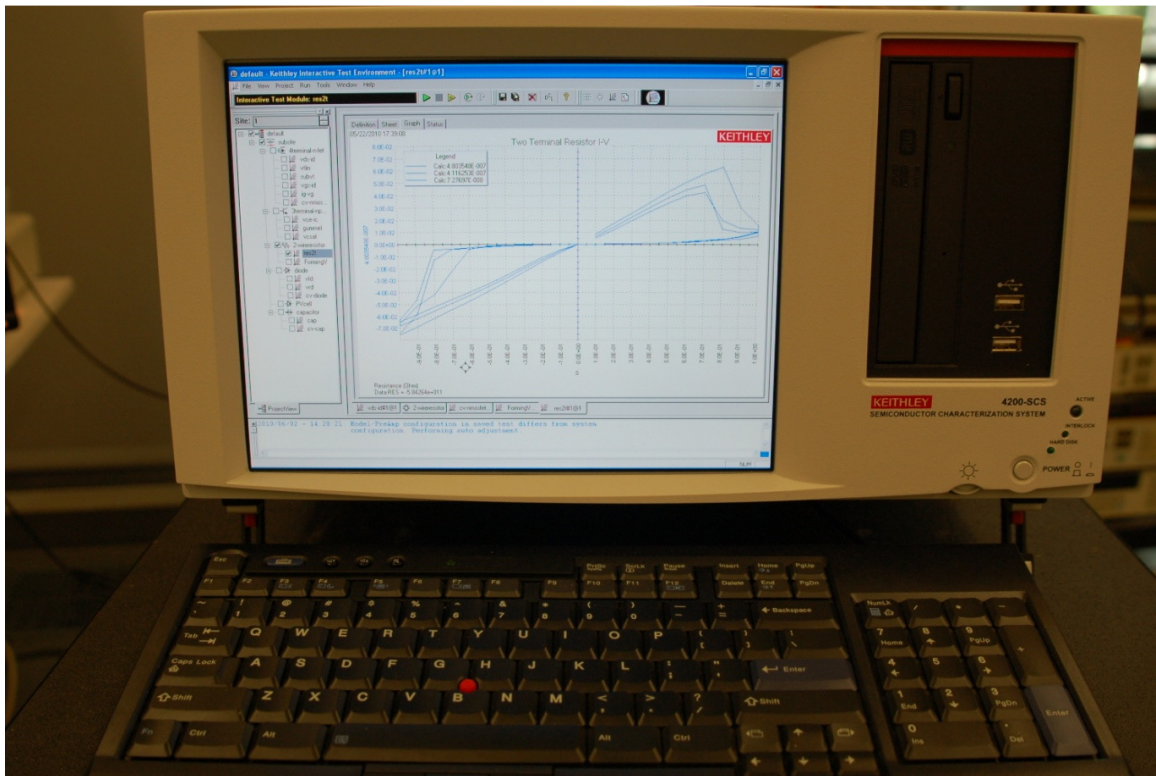


Figure 11. Keithley 4200 Semiconductor Characterization System.

succession so that the difference between each curve is more apparent and the hysteresis effect of the memristor is easily observed.

3.4 Modeling

The first step in modeling the memristor was to take the equations from Strukov et al. [1], and implement them in a Matlab model. This models the most ideal case and is useful for some insight into the behavior of the memristor. ODE45 was the Matlab function utilized in order to realize the ideal model. The actual code and discussion of how well the ideal model worked are discussed under the results chapter.

The next step after fabricating some actual memristors using anodization was to model these memristors in Cadence so that simulations could be done on some innovative circuits implementing memristors. It was easy enough to use VerilogA to model the ideal memristor. Unfortunately, real memristors are affected by the boundaries of the switching medium and therefore see non-linear dopant drift. Joglekar [12] used a windowing function to model this non-linear drift behavior, and this windowing function just needed to be added to the Cadence VerilogA code.

$$\frac{dw}{dt} = \frac{\mu_V R_{ON}}{D} i(t) * F\left(\frac{w}{D}\right) \quad (14)$$

$$F\left(\frac{w}{D}\right) = 1 - \left(2\frac{w}{D} - 1\right)^{2p} \quad (15)$$

The equations above show the original vacancy drift over time equation with the windowing function multiplied by it. Using all the process dependent variables: μ_v , R_{ON} , R_{OFF} , p , D , and w ; it should be possible to create a satisfactory model of the memristors created in this work. Unfortunately Cadence responded to the windowing function with convergence errors that have not been fixed. Nevertheless, the VerilogA code created thus far is included in Appendix B.

A SPICE model from Biolek et al. [13] was used without modification in ORCAD PSPICE Lite 9.2. Using this model, a decent representation of the memristor with non-linear dopant drift taken into account was realized. The results of using this model to imitate memristors created through anodization is explained in the next chapter.

3.5 Summary

Memristors were fabricated by taking a thin film of titanium deposited on a glass slide and anodizing a small area. The titanium bottom contact and silver paste top contact with TiO_2 in between form the 2-terminal device. Two sets of these devices were made and one set was annealed for comparison. This device will be subjected to a “figure-8” test and a “soft-switching” test after applying a necessary forming voltage. Once memristive behavior has been observed, a Pspice model will be used to match the behavior of the real sample. The results of all the methods described are covered in-depth in chapter 4.

CHAPTER 4. RESULTS

4.1 Keithley Measurement Results

The “figure-8” sweep was completed first. Ideally, the current-voltage characteristics would be symmetric about the origin and have two very distinct slopes. The shallow slope defines the high resistance state and the steep slope the low resistance state.

Fig. 12 displays a “figure-8” measurement from each sample that was not annealed. The magnitude of the measured current varies from one sample to the next up to an order of magnitude. To provide a clear comparison between the various samples, the measured current for each sample was normalized by the maximum value for that particular sample. The N above each plot just designates these results as the samples that were not annealed, and the number after N is anodization time. It is clear that the samples demonstrate the bias dependent bipolar switching characteristics indicative of memristors, as opposed to the filament controlled unipolar switching characteristics of fuse-antifuse type resistive memory elements [4]. Also, with the exception of sample N60, all samples have a high degree of symmetry with respect to the origin. Differences do exist in the normalized conductivity of the respective high- and low- conductivity states (here onwards referred to as the ON and OFF state, respectively).

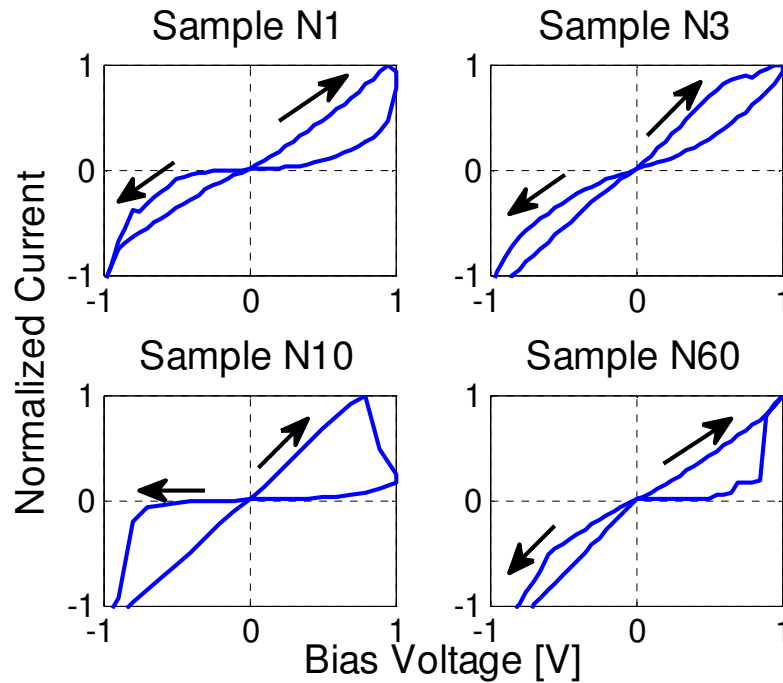


Figure 12. Samples that were not annealed. The number above each plot states how many seconds the sample was anodized for. All currents have been normalized and arrows denote the direction of the sweep.

The normalized conductivity of the ON and OFF state for sample N1 is 890.2 mS and 61.6 mS, respectively. The normalized conductivity of the ON and OFF state for sample N3 is 1.231 S and 438.5 mS, respectively. The normalized conductivity of the ON and OFF states of sample N10 is 1.2560 S and 22.4 mS, respectively. The conductivity of the ON and OFF state could not be accurately estimated for sample N60 due to asymmetric I-V characteristic.

The annealed samples experienced no memristive behavior and only slight Schottky barrier curves shown in Fig. 13. This is because there are already some oxygen vacancies at the Ti-TiO₂ barrier since some oxygen will leave the TiO₂ to oxidize Ti near the junction [6]. These oxygen vacancies were enough to create memristive behavior as demonstrated with the samples that were not annealed. Applying a positive bias to the Ti in this case would repel

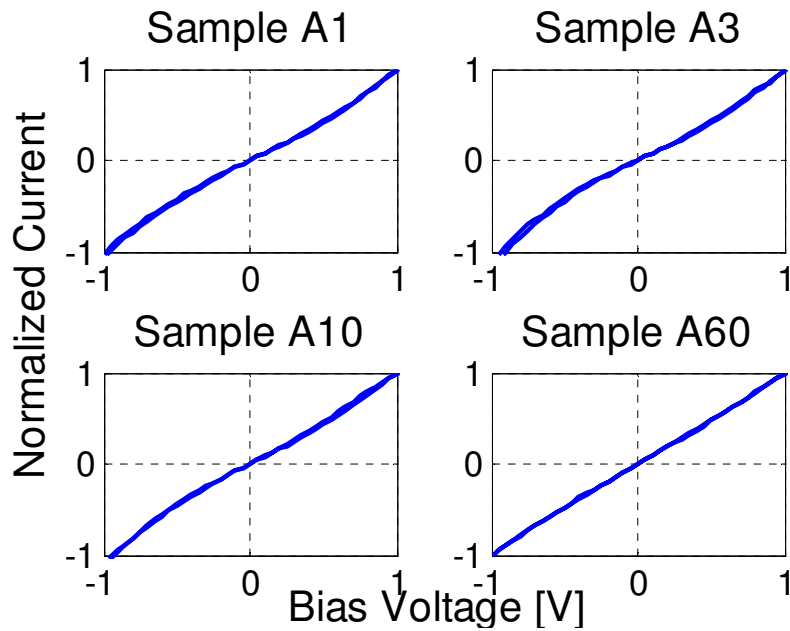


Figure 13. Annealed samples. The anodization time for each sample is above the respective plot. All currents have been normalized.

the oxygen vacancies eventually shorting the Schottky barrier at the silver paste and TiO_2 junction. Annealing the samples created oxygen vacancies at the silver paste and TiO_2 junction, so both junctions are now ohmic, and there cannot be any switching behavior.

The reproducibility of the memristive switching characteristics was also studied. Fig. 14 shows three consecutive sweeps for sample N10. The sweep rate was mentioned above and while it was not tested, it is expected that the curves in Fig. 14 would collapse to resemble the curves in Fig. 13 if the sweep rate were to be greatly increased [1].

All other non-annealed samples showed similar levels of reproducibility when consecutive measurements were taken at the same spot as well as when measurements were taken at different points on the sample. Slight variations in the current levels across different sweeps, as seen in Fig. 14, are expected and have been previously observed (e.g., [6]). The current flowing through the memristor is higher than previously reported devices (e.g., [1],

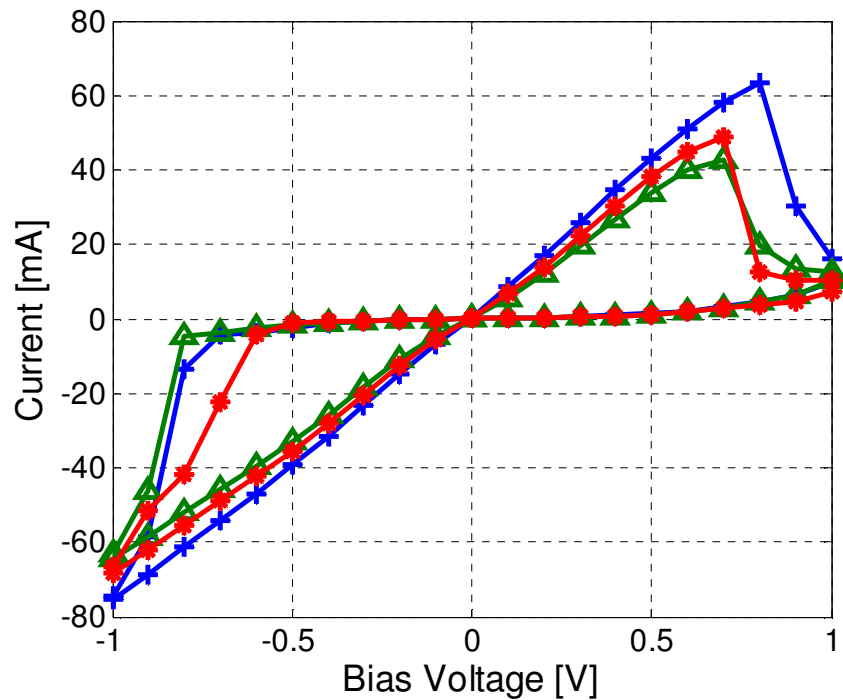


Figure 14. Three consecutive sweeps on the not-annealed ten second sample.

[6]), but this is due to the larger cross-sectional area of our devices ($\sim 1 \text{ cm}^2$ as compared to $\sim 2500 \text{ nm}^2$ for the devices in [6]).

“Soft-Switching” proves memristance in a sample because the sweep does not go negative allowing observation of the “memory” of the memristor. Each sweep is expected to be higher than the last due to higher current as the device loses resistance and approaches the ON state. Fig. 15 displays the results for the samples not annealed. Once again the anodization times are above each plot and the currents are normalized to the maximum current for that particular sample. The blue line is the first sweep and the green line is the sixth sweep. If the other sweeps were depicted, you would see them continually rising between the first and sixth sweep. All the samples in Fig. 15 demonstrate memristive behavior, but N10 and N60 show a curve that is similar to a Schottky rectifier. Sample N1

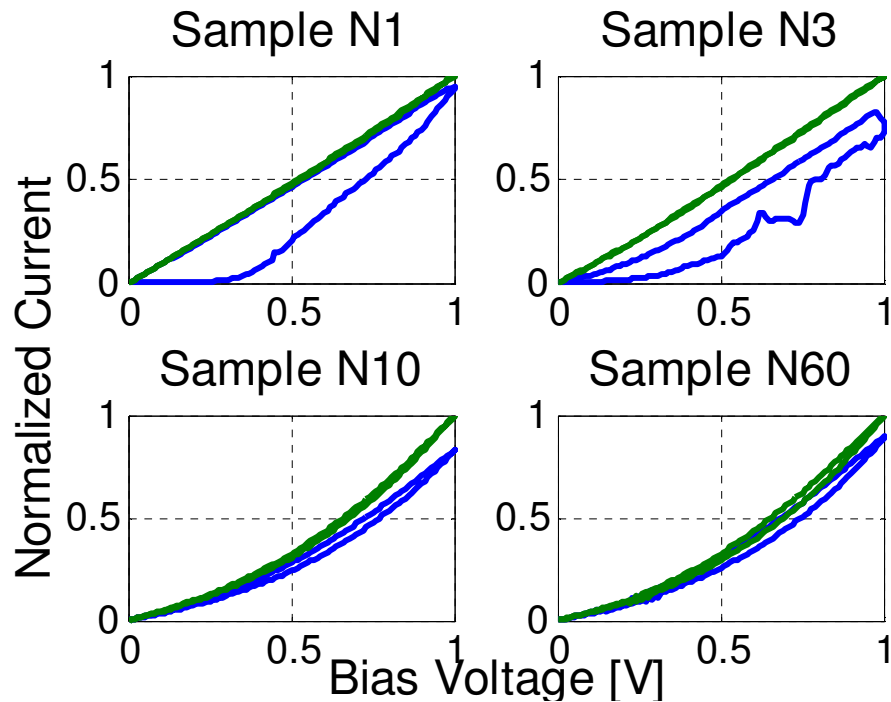


Figure 15. "Soft-Switching" sweeps for the not-annealed samples.

shows almost no separation between the first and sixth sweep and looks to have been completely switched to the ON state after the first sweep.

Fig. 16 presents the "soft-switching" results for the annealed samples. All the samples show little memristive behavior in that the differences between the first and sixth sweep are negligible. A3 is the only sample that shows a substantial difference, but the plot is very erratic. Once again, because both the TiO_2 -silver paste and TiO_2 -Ti contacts are ohmic, very little memristive behavior is observed.

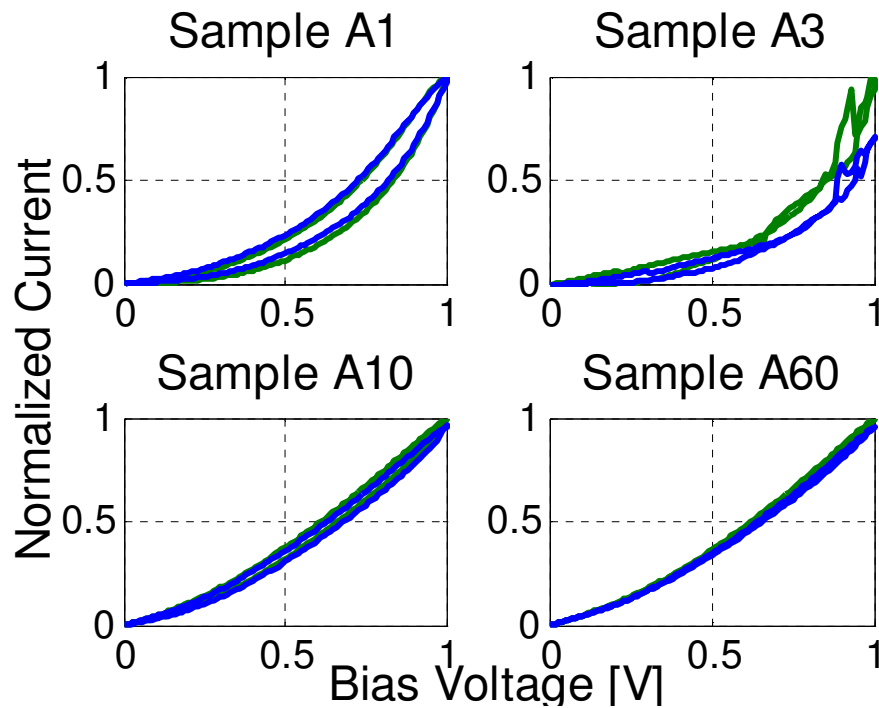


Figure 16. "Soft-Switching" sweeps for annealed samples.

4.2 Atomic Force Microscopy Results

Atomic Force Microscopy (AFM) uses a sub-nanometer probe to scan the surface of a sample record the deflections of the tip. This results in the images in Fig. 17 which represent height-maps of each sample that was not annealed. The bright yellow color represents an area of high elevation while darker yellow represents low elevation. From the pictures it can

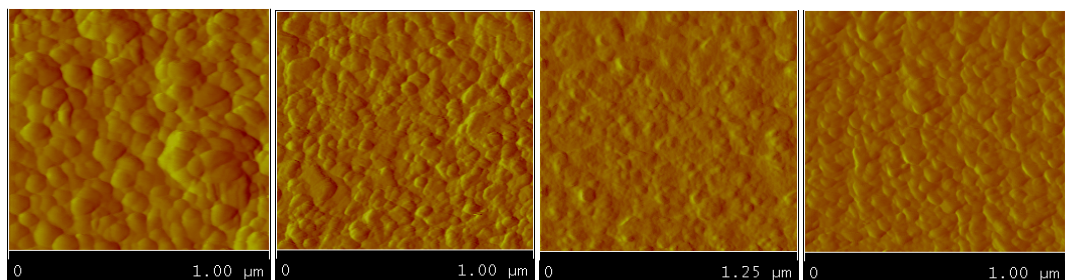


Figure 17. AFM images for not-annealed samples. Left to Right: 60s, 10s, 3s, 1s.

be concluded that as the sample is anodized for a longer period of time, the surface of the sample averages out and becomes smooth. The electrolyte mixture used for anodization is meant to grow tubes of TiO_2 [20], but it is clear that the etching process for the growth of the tubes has not started yet even in the sixty second sample.

4.3 Ideal Matlab Modeling Results

Modeling the ideal memristor in Matlab proved not very difficult, and it was possible to achieve plots that looked identical to the plots found in Strukov et al. [1]. Two separate models were created, one that took the current as an input and solved for the voltage just like the equations posited in [1]. The other model took the voltage as an input and solved for the current. Both models did a good job of showing the ideal properties of the memristor, but it was easy to have w less than 0 or greater than D which was unrealistic as explained in 2.1. A bounding function was added that simply replaced any values of w with 0 or D appropriately and then calculated the resulting current or voltage. This still came out with unrealistic results. Fig. 18 shows a plot made with the final version of the Matlab memristor model, and the code used for this final version is displayed in Appendix A.

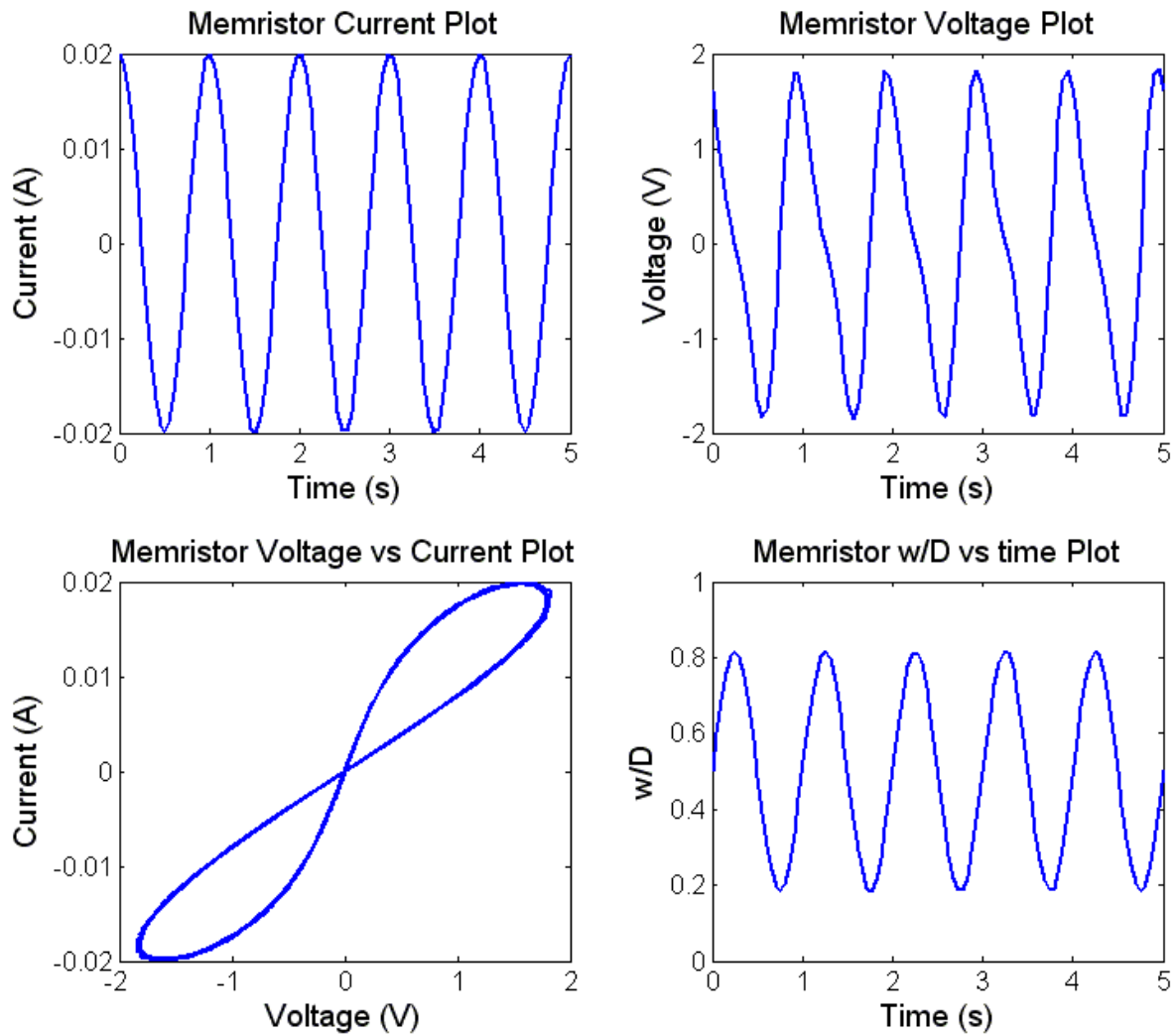


Figure 18. Plot made with Matlab memristor model.

4.4 ORCAD Pspice Memristor Model

As stated before, the model used is from Biolek et al. [13] with no modification. The process parameters contained in the model were tweaked in order to match the beautiful ten second sample curves shown in Fig. 14.

$$\frac{dw}{dt} = \frac{\mu_V R_{ON}}{D} i(t) * \left(1 - \left(\frac{2w}{D} - 1 \right)^{2p} \right) \quad (16)$$

$$v(t) = \left(R_{ON} \frac{w(t)}{D} + R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right) i(t) \quad (17)$$

The above equations show the main equations used in the model to determine the behavior of the memristor device. The direct values calculated from the slopes of the ten second curves for R_{OFF} and R_{ON} were used. The mobility μ_V was considered fixed as the drift of oxygen vacancies is known [1]. The time the sample was anodized is known but the thickness, D , is unknown. Because of this, D was considered a variable to help fit the ten second device curve. Other variables for fitting were R_{INIT} and p . In order to mimic the testing conditions applied to the ten second sample, a voltage source that took time and voltage points from a file was employed. The file was set up with three DC sweeps identical to the Keithley with about 8 seconds per sweep and a few seconds in between each sweep. The final values used for all the parameters are displayed in Table 1.

The final value for D ended up being a bit thick, but until AFM results are able to confirm the thickness of the oxide for each sample, this could be the actual thickness of the ten second sample. R_{ON} is the exact on resistance calculated from the slope of the ten second

Table 1. Memristor parameters used for Pspice model .

Memristor Parameters Used for Pspice Model	
D	90 nm
R_{INIT}	170 Ω
R_{ON}	12 Ω
R_{OFF}	800 Ω
μ_V	10 fm ² /(Vs)
p	10

sample, but R_{OFF} was doubled from its original value. The reason for this could be explained by the gross non-linearity seen in the slope as the memristor approaches the “ON” state. The “OFF” state was calculated by fitting a straight line to this non-linear curve, so it is reasonable that the calculated value of R_{OFF} could be far off from the actual value. R_{INIT} was the most important variable for matching the curve to the ten second. This variable determines the starting resistance of the model, or where the function $w(t)$ starts in relation to D . With the parameter setup and voltage source described the following plots were created.

Comparing the model to the measured curves depicted in Fig. 19, it is clear that there are many similarities. The magnitude of the current is close and the shape of the positive curve is also very close. Even the collapse from the first to the second sweep looks similar

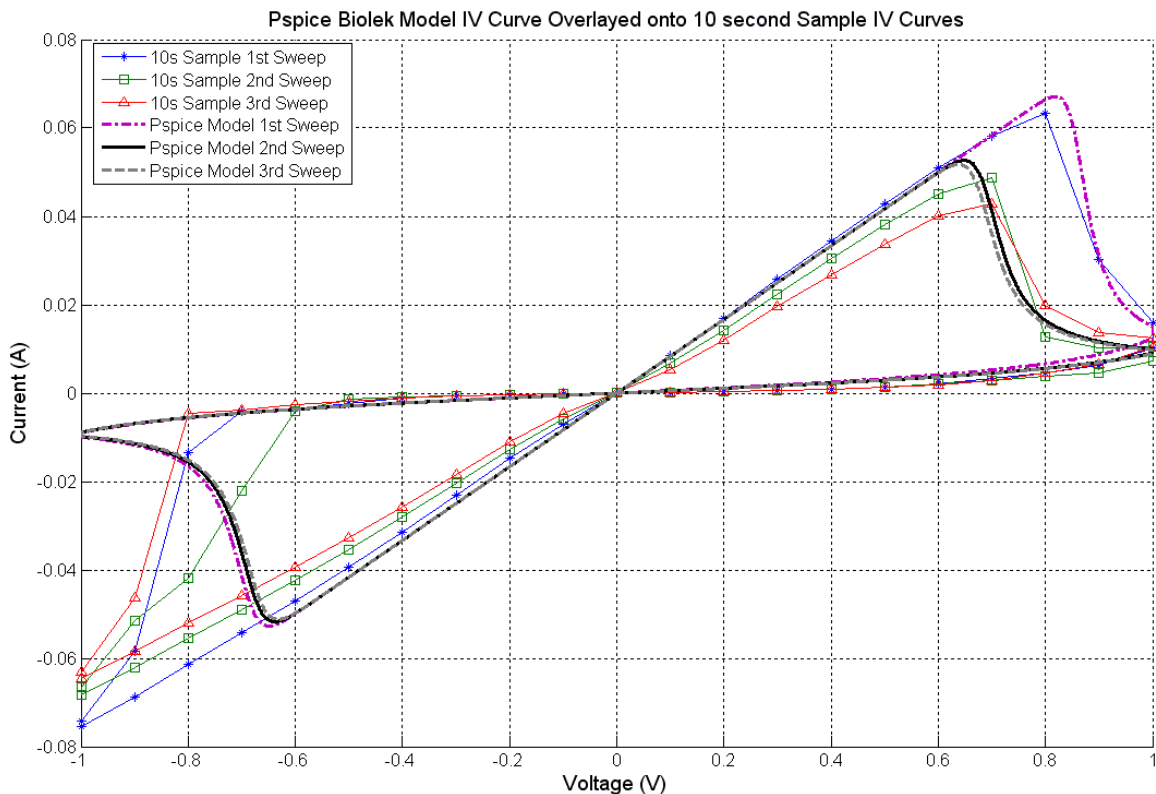


Figure 19. Comparison of Biolek Pspice model to 10 second sample.

and the negligible collapse between the second and third sweep is mimicked. Most of the differences appear on the negative side of the plot. The outward spike on the curve is on the top of the curve instead of the bottom like the ten second sample. The model would have to be changed to get this large difference correct as the model currently makes both sides highly symmetric. The current magnitude is not quite high enough on the low side and seems to saturate around -50 mA where the high side saturates around +80 mA. The collapse between each sweep on the negative side is in line with the ten second sample in that there is little change. Despite the shortfalls in the model, the representation is very good. Fig. 20 displays the voltage versus time while Fig. 21 shows the current versus time of the same test.

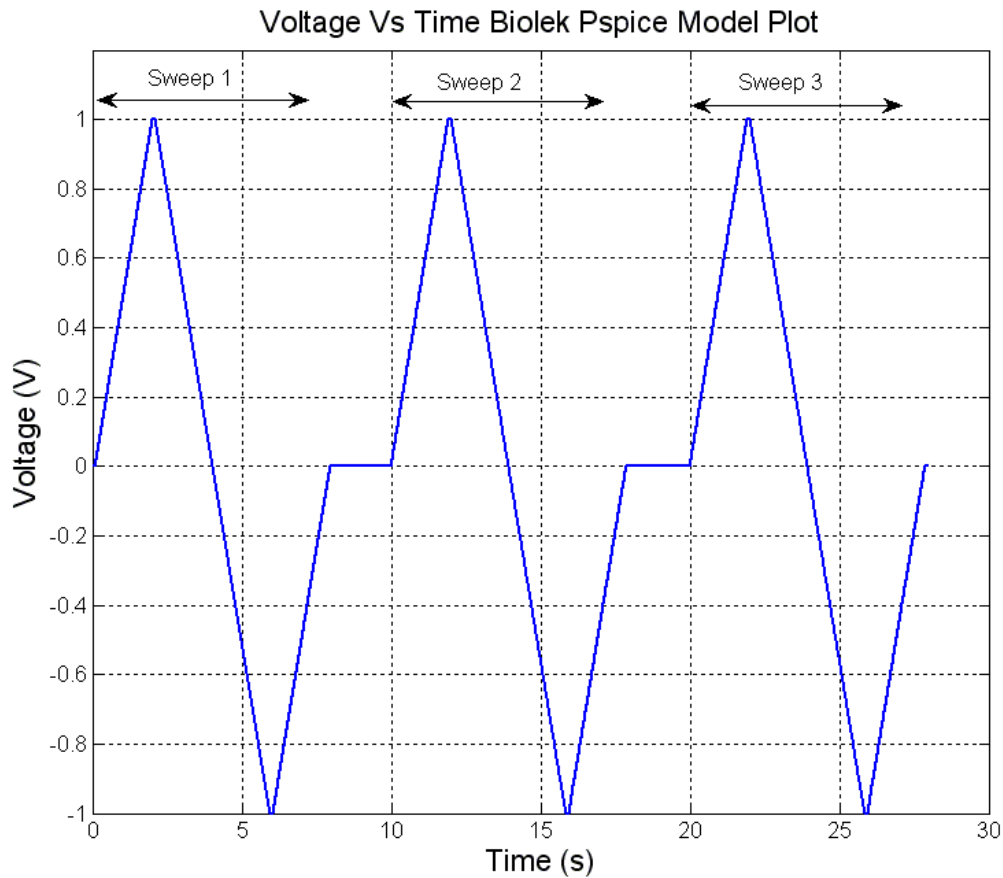


Figure 20. Pspice V vs time memristor model curve.

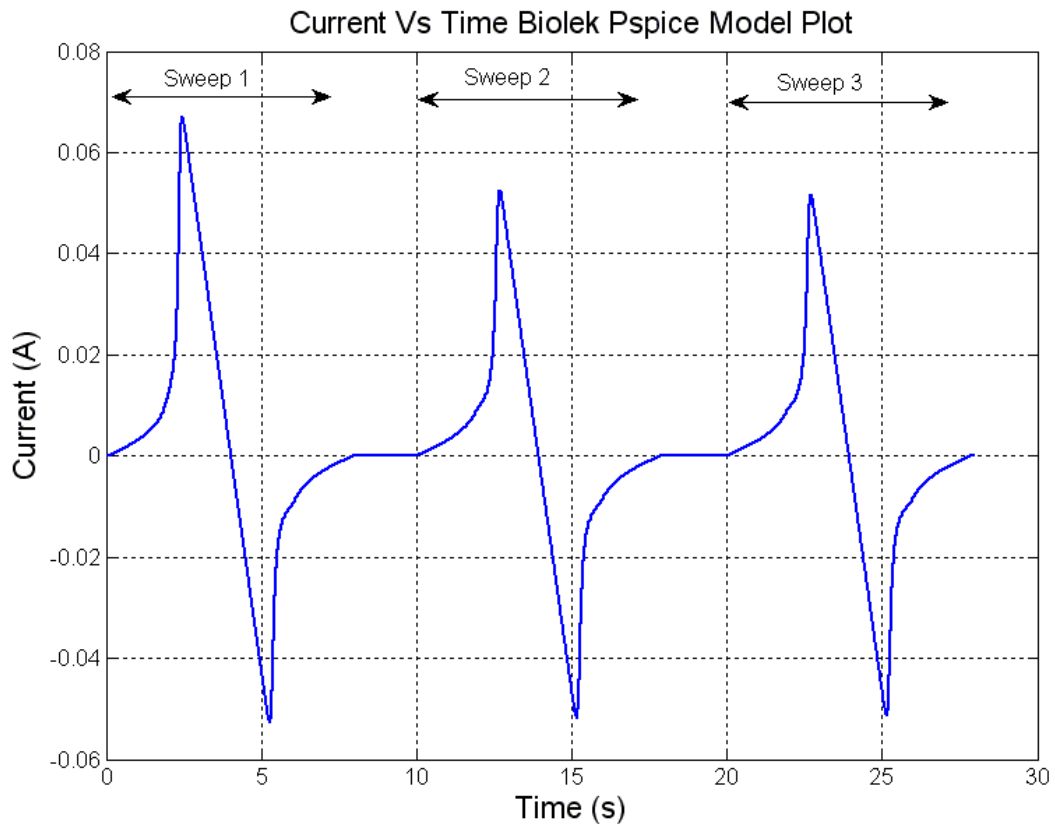


Figure 21. Pspice I vs time memristor model curve.

4.5 Summary

Using the Keithley to apply a “figure-8” and “soft-switching” sweep to each anodic titania sample yielded interesting results as described in Section 4.1. Memristive behavior was showcased on the samples that were not annealed while the annealed samples generally produced linear resistive behavior. This was explained by the fact that at the Ti-TiO₂ interface oxygen vacancies will be created inherently because of some oxygen escaping to oxidize the titanium at the boundary. The concentration seemed to be large enough to make this metal-semiconductor junction ohmic. This junction is inside the sample and not exposed, so when the samples were annealed, the very top of the oxide was reduced creating

oxygen vacancies. Since the annealing affected the other junction, both contacts became ohmic in the annealed case causing the devices to act mostly like resistors.

The early ideal modeling with Matlab was good to obtain a deeper understanding of how the memristor operates, but the real goal of modeling was to imitate the samples. Utilizing the Pspice model proposed in Biolek et al. [13], parameters were presented that characterize the best sample.

CHAPTER 5. FUTURE WORK

5.1 Memristor Fabrication

Although the concept of creating a memristor using anodization has been proven, there are many directions in which to proceed. Different materials could be anodized to see if they also exhibit memristive behavior. A new electrolyte could be tried that does not contain the fluoride for growing the TiO_2 nanotubes [20]. The directions being explored now or in the near future are AFM analysis, varying anodization times, and fabricating on a substrate of TiO_2 .

Some AFM was completed on the first set of samples, but was largely inconclusive. It was obvious in the AFM pictures that height gradients evened out as the anodization times increased, and that nanotubes were not forming yet, but not much else could be concluded. New samples have been fabricated just for CAFM in order to confirm what drives conduction in the anodic titania memristor.

Trying different anodization times could bring better understanding for how thick of an oxide it takes to create the best memristor and produce more data for characterizing the thickness of oxide grown. Specifically times above two minutes would be most favorable as these times have not yet been tested. At these longer anodization times it will be interesting to observe the memristance decrease as the thickness increases as well as investigating what kind of affect the nanotube structures have on the memristor device as they start to form.

Procuring a TiO_2 substrate will enable the creation of memristors much like what has already been created in previous work. The fabrication then will not be novel, but these

devices should be more reliable and have a higher yield allowing more experimentation to be done in other areas that could not be started due to the infancy of the current anodic memristors. Temperature characterization would be a viable next step with reliable devices as well as investigating simple memristor circuits created on a breadboard.

5.2 Memristor Modeling

Little has been done on the modeling front thus far leaving much yet to be done. The new model from Kavehei, et al. [15], would be best if implemented in Cadence either as a VerilogA or SPICE macro model. This would allow the research group to start improving old circuit designs and designing new circuits capitalizing on the properties of the memristor. Since the memristor model is still in its infancy, there is also the opportunity to improve on existing models especially if a reliable device is created to base the model on.

5.3 Summary

Memristor research at Iowa State is off to a good start. As explained in chapter 5, the future possibilities for memristor research are wide open given how new the field is. It was a pleasure to have the opportunity to start research in this area, and it will be an even greater pleasure to see future students build on this thesis and take the research to new heights.

APPENDIX A: MATLAB MEMRISTOR MODEL CODE

A.1 Main Body of Code

```

function memristor_ode_solver(tspan, points, Amp, freq, Ron, Roff, D, uV,
bounds)
% Author: Kyle Miller
% This models a memristor using a cos current input to solve for the
% voltage
%
% memristor_ode_solver(tspan, points, Amp, freq, Ron, Roff, D, uV, bounds)
%
% inputs:
% tspan      Vector with initial and final time: [t0 tf]
% points     Integer number specifying how many equally spaced points
%            between the initial and final time to be evaluated
% Amp        Amplitude of current input (For best results use around 0.02)
% freq       Frequency of current input (Use 1 to see figure 8 curve)
% Ron        Resistance of memristor when "On" (1)
% Roff       Resistance of memristor when "Off" (160)
% D          length of memristor (10e-9)
% uV         mobility of oxygen vacancies (10e-15)
% bounds     1 if w should be bounded from 0 to D, 0 if not (Optional,
%            default is 0)

% Check if Optional arguments given
if exist('bounds') == 0
    bounds = 0;
end

% Create vector of initial values
w0 = 0.5*D;

tspan = linspace(tspan(1),tspan(2),points);

% Solve dw/dt assuming i(t) = A*cos(wt)
[t, w] = ode45('memristor', tspan, w0, '', Amp, freq, Ron, Roff, D, uV);

% correct the w vector according to bounds [0 D]
if bounds == 1
    for i=1:length(t)
        if w(i) < 0
            w(i) = 0;
        elseif w(i) > D
            w(i) = D;
        end
    end
end

% Find the current
I = Amp*cos(freq*2*pi*t);

```

```

% Find the voltage
V = (Ron*w/D+Roff*(1-w/D)).*Amp.*cos(freq*2*pi*t);

subplot(2,2,1);
plot(t,I)
title 'Memristor Current Plot';
xlabel 'Time (s)';
ylabel 'Current (A)';

subplot(2,2,2);
plot(t,V)
title 'Memristor Voltage Plot';
xlabel 'Time (s)';
ylabel 'Voltage (V)';

subplot(2,2,3);
plot(V,I)
title 'Memristor Voltage vs Current Plot';
xlabel 'Voltage (V)';
ylabel 'Current (A)';

subplot(2,2,4);
plot(t,w/D)
title 'Memristor w/D vs time Plot';
xlabel 'Time (s)';
ylabel 'w/D ()';

```

A.2 ODE45 Function Code

```

function dwdt = memristor(t,w,flag,Amp,freq,Ron,Roff,D,uV)
% Author: Kyle Miller
% This models the W of a memristor
%
% inputs:
% t      time
% w      initial value of w

% Assuming current is A*cos(w*t)
dwdt = uV*Ron/D*Amp*cos(freq*2*pi*t);

```

APPENDIX B: VERILOGA MEMRISTOR CODE

```
// VerilogA for Research, IdealMemristor, veriloga

`include "constants.vams"
`include "disciplines.vams"

module IdealMemristor(p, n);

input p;
output n;
electrical p, n;

parameter real Roff = 160;
parameter real Ron = 1;
parameter real D = 10n;
parameter real uv = 10f;
parameter real w_init = 5n;
parameter real x = 10; // Windowing function coefficient

real w;

analog begin

    @(initial_step) begin
        w = w_init;
    end

    // Original Model, linear dopant drift
    ///////////////////////////////////////////////////////////////////
    // May want to add initial condition and RESET in idt
    // idt(expression, ic, reset)
    w = uv*Ron/D*idt(I(p,n), w_init);

    // Models with nonlinear dopant drift
    ///////////////////////////////////////////////////////////////////
    //w = uv*Ron/D*idt(I(p,n)*(1-pow(2*w/D-1, (2*x))), w);

    V(p,n) <+ (Ron*w/D+Roff*(1-w/D))*I(p,n);

end

endmodule
```

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